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# Controller for the Electronically Scanned Thinned Array Radiometer (ESTAR) Instrument

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***Abstract:*** *A prototype Controller for the ESTAR (Electronically Scanned Thinned Array Radiometer) instrument has been designed and tested. It manages the operation of the Digital Data Subsystem (DDS) and its communication with the Small Explorer Data System (SEDS). Among the data processing tasks that it coordinates are FEM data acquisition, noise removal, phase alignment and correlation. Its control functions include instrument calibration and testing of two critical subsystems, the Output Data Formatter and Walsh Function Generator. It is implemented in a Xilinx XC3064PC84-100 Field Programmable Gate Array (FPGA) and has a maximum clocking frequency of 10 MHz.*

## 1. Introduction

ESTAR (Electronically Scanned Thinned Array Radiometer) is a passive synthetic-aperture radiometer designed to sense soil moisture and ocean salinity in L-band. It is being developed as an earth probe mission intended for launch in the late 1990's as part of the Earth Observing System (EOS).

A recent feasibility study [1] of the ESTAR concept recommended that a two-dimensional prototype be built in order to study further the design issues involved. Grand Valley State University School of Engineering has undertaken the task of designing and building four subsystems that will be part of the Digital Data Subsystem (DDS) in this prototype. The last of these subsystems, the DDS Controller, has been completed and is the subject of this memorandum. Three previous memoranda [2,3,4] present the specifications of the other subsystems, called the Output Data Formatter (ODF), Walsh Function Generator (WFG) and Phase Aligner (PA).

Section 2 is a presentation of background information about the ESTAR. Sections 3 presents the operation and design details of the DDS Controller, and Sections 4, 5 and 6 contain the specifications of the design.

## 2. ESTAR Background

The synthetic aperture sensing technique employed by ESTAR is a method whereby the high spatial resolution and sensitivity of a large dish antenna can be duplicated with a small, lightweight cross-shaped array of dipole antennas (see Figure 1).

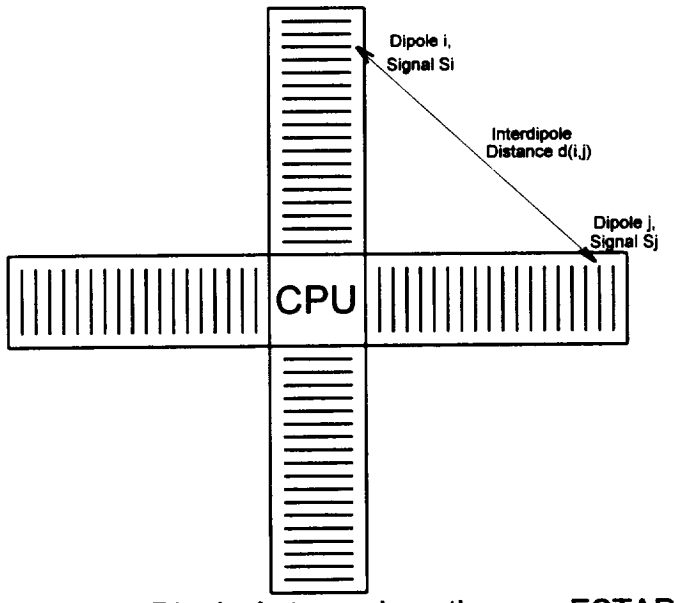



Figure 1: Dipole Antenna Locations on ESTAR

Such a duplication yields size and weight advantages which make it attractive for use on earth-sensing spacecraft. It is made possible by the calculation, for all pairs (i,j), of the pairwise complex correlation between dipole signals $S_i$ and $S_j$ using the formula

$$< S_i, S_j >= \frac{1}{T}\int_0^T S_i(t)S_j^*(t)dt \ , \qquad (1)$$

in which "*" denotes the complex conjugate and T is a suitably chosen integration period. It can be shown that each of these correlations is a sample, in frequency space, of the spatial Fourier Transform of the brightness temperature distribution over the field-of-view (FOV) of the antenna. Consequently, the visibility function in the FOV can be computed by inverting the sampled transform. Furthermore, the location of the sample in frequency space is determined only by the inter-dipole distance and not by the absolute locations of the dipoles themselves [5].

The data processing system on ESTAR will compute, in real time, these correlations for each dipole pair (i,j). Sensitivity and resolution specifications dictate that 145 dipoles (73 on each leg of the cross) must be used for a full ESTAR mission, or 73 (37 on each leg) for a reduced mission [6]. The correlations will be done digitally at a centrally located processing unit called the CPU, as shown in the figure. The results will then be sent to earth where the inverse transform will be computed. Necessary dipole signal preprocessing, including down-mixing and A/D conversion, will be done at each dipole by circuitry contained in a "Front End Module" (FEM).

### 2.1 Major Digital Data Subsystem Components

At the functional level, the Digital Data Subsystem (DDS) consists of six major components [7]. The first of these, the Digitizer, must convert the FEM data to digital form before sending it to the CPU. This will be done by an A/D converter in each FEM. The second, the Data Bus, must transport the digitized data from the FEMs to the CPU. The third, the CPU, must compute the correlations for each pair of FEMs. It is also responsible for overall management of the DDS. Furthermore, it must interface with the Small Explorer Data System (SEDS), which is a software and hardware "operating system" on the space vehicle. Among other tasks, SEDS performs overhead functions such as error-coding and transmission to earth, earth command processing and system test. The CPU must pass the correlation products to SEDS for transmission to earth.

The fourth component, the System Clock, is necessary to ensure that dipole data samples are generated synchronously by all FEMs. In effect, the Clock signals the FEMs to generate data samples at the same instant of time. The fifth part, the Phase-Aligner (PA), removes the phase differences between FEM samples when they arrive at the CPU. These differences are caused by unequal data propagation times to the CPU from distant and nearby FEMs. The PA must hold the early-arriving data until the late-arriving data is available. Only when all FEM data for a particular sample time have arrived at the CPU will the PA signal the CPU that the data is ready for correlation. The sixth component, the Walsh Function Generator (WFG), generates a unique Walsh function signal for each FEM. This signal is

used to cancel low frequency noise generated by the analog circuitry in the FEM. These six components fit together as shown in Figure 2.

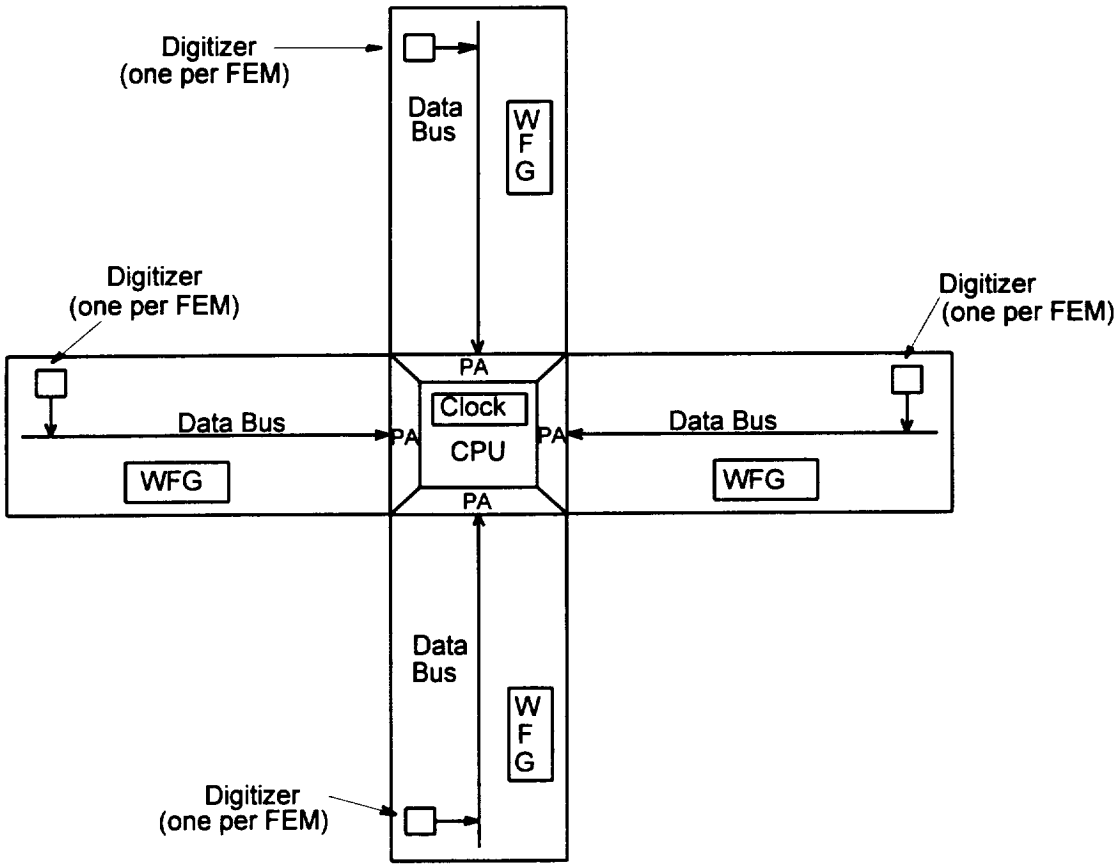



Figure 2: Six Major Components of the DDS

The CPU consists of three major components. The Correlator computes product (1) and is an ASIC developed by the NASA Space Engineering Research Center at the University of New Mexico. The Output Data Formatter (ODF) provides the data interface to SEDS, which involves location-stamping of the correlation products before transmission to earth [2]. The DDS Controller performs DDS management and is the subject of this memorandum.

## 2.2 DDS Controller Requirements

The DDS management task involves both DDS control and SEDS communication functions. The former involves the control of the data bus, PA, ODF, Correlator and WFG during five modes of operation: correlate, output, calibrate, command and test. The latter involves command interpretation and status provision.

### 2.2.1 DDS Control

Correlate mode involves computation in the Correlator of the digitized data stream from the FEMs. During output mode the results are input to the ODF for passage to SEDs. Calibrate mode represents a "sanity check" for the instrument. It is the same as the correlate mode except that the signals for the dipole antennas are derived from locally generated calibration sources. Command mode is a "resting" state in which the Controller awaits a command from SEDS. Once a command arrives it is decoded and further action, such as entering another mode, is taken. Test mode involves the exercise of the ODF and WFG (using their internal test circuitry) as well as the interpretation and communication of the results to SEDS.

The mode of the DDS is continuously cycled through the sequence correlate, output, calibrate and output. In this way the drift of the analog circuitry in the FEMs can be continuously eliminated during earth processing. This sequence can be interrupted only by entering command mode. As will now be discussed, the DDS can then remain in command mode (reset command) or enter test mode (test command).

### 2.2.2 SEDS Communication

The possible SEDS commands are reset, test, proceed and data received. Reset instructs the Controller to reset the PA, ODF, WFG and Correlator, and to await a subsequent command. Test tells the Controller to enter Test mode, during which the ODF and WFG are exercised in order to determine their degree of functionality. This command requires the specification of an identification code which tells the Controller which of the Walsh Function Generator chips to test and will be discussed in Section 3. Proceed is a "null" command which causes the Controller to continue its normal sequence of operation. Data received is asserted to tell the Controller that SEDS has received the correlation products from the ODF and is ready for more.

The status of the DDS is communicated to SEDS using one of the six conditions in-reset, proceeding, testing, error-in-ODF, error-in-WFG and data-is-available. In-reset and testing exist respectively after reset or test commands are being executed. The proceeding condition exists during the "normal" sequence of modes correlate, output, calibrate, output discussed above. The error status conditions tell SEDS that a malfunction has been detected in the corresponding subsystem. Data-is-available instructs SEDS that a correlation product is available.

The remainder of this memorandum is as follows. Section 3 presents the details of the Controller design. Section 4 contains its specifications. Sections 5 and 6 contain signal descriptions and implementation statistics, respectively.

## 3. Controller Design

### 3.1 General Description

The DDS Controller prototype is depicted in Figure 3, where the signals have been

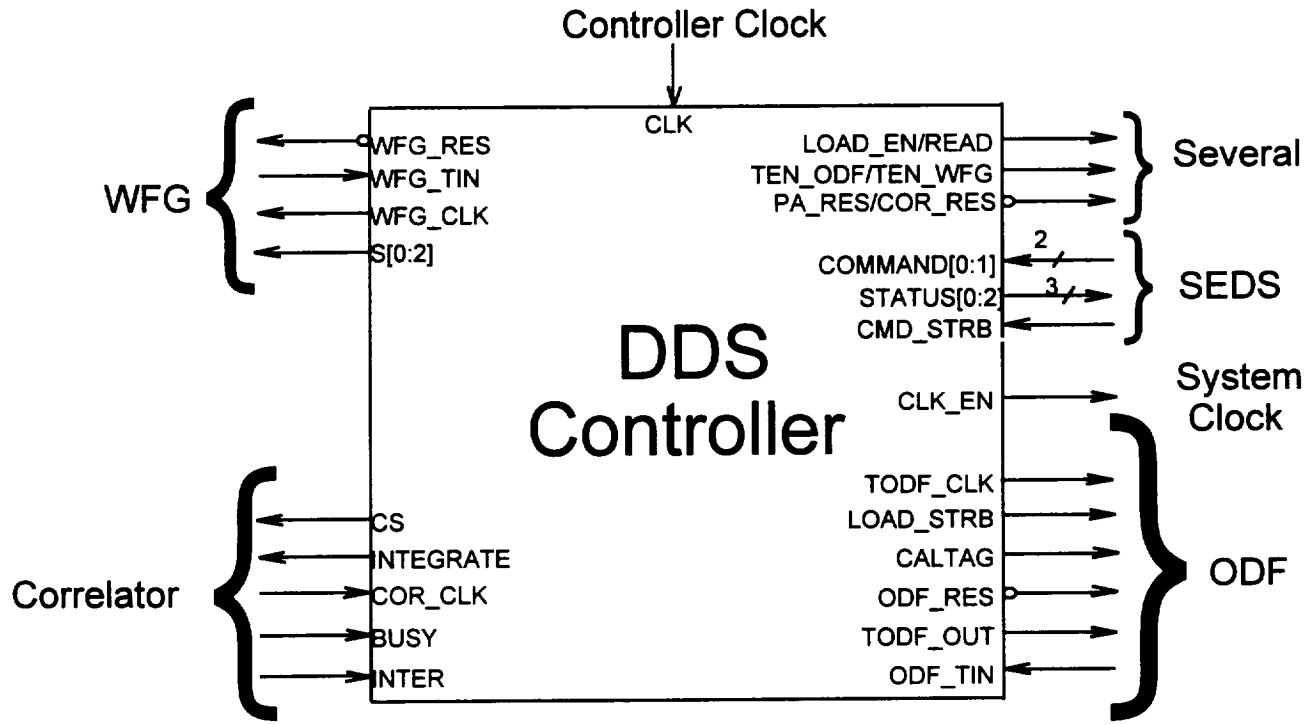



Figure 3: DDS Controller Signals

grouped according to the subsystem in which they are used.

CLK_EN is the enable signal for the System Clock (not shown). The clock produces two system clocking signals: COR_CLK for the Data Bus, PA and Correlator and CLK for the Controller and the remainder of the DDS. The frequency of COR_CLK must be twice that of CLK.

The signals for the WFG are a clock (WFG_CLK), enable (WFG_RES), test data input (WFG_TIN) and three outputs (S[0:2]) which indicate the particular WFG device that is to be examined by specifying the 32 function set that will be generated during the test. The data on the S[0:2] outputs are the identification code received from SEDS as part of the test command. This is discussed in Section 2.

The ODF signals include a load (LOAD_STRB), calibration mode indicator (CALTAG), enable (ODF_RES), test clock (TODF_CLK), test data source (TODF_OUT) and an input for test results from the ODF (ODF_TIN). More information about the WFG and ODF can be found in the technical memoranda describing their design [2,3].

The Correlator signals include chip select/Correlation product output strobe (CS), correlate (INTEGRATE), clock (COR_CLK), active indicator (BUSY) and data ready indicator (INTER).

Multi-subsystem signals include LOAD_EN/READ, which enables data output from the Correlator and data input to the ODF, a test enabling signal for the ODF and WFG (TEN_ODF/TEN_WFG), and the enable for the PA and Correlator (PA_RES/COR_RES). Input CLK is the clock signal for the Controller.

The SEDS signals include a data output strobe (CMD_STRB), status signals (STATUS[0:2]), and a command input (COMMAND[0:1]). The commands and status bits were discussed in Section 2. The truth tables are shown in Tables 1 and 2.

Table 1: Command Bit Truth Table

| | COMMAND1 | COMMAND0 |
|---|---|---|
| RESET | 0 | 0 |
| TEST | 0 | 1 |
| PROCEED | 1 | 0 |
| DATA_RCVD | 1 | 1 |

Table 2: Status Bit Truth Table

| | STATUS2 | STATUS1 | STATUS0 |
|---|---|---|---|
| RESTAT | 0 | 0 | 0 |
| TESTING | 1 | 0 | 0 |
| ERRODF | 1 | 0 | 1 |
| ERRWFG | 1 | 1 | 0 |
| PROCEEDING | 0 | 1 | 0 |
| DATAVAIL | 0 | 1 | 1 |

### 3.2 Circuit Operation

Operation of the DDS Controller prototype will now be described. At power-up the Controller is in command mode, staring at the COMMAND[0:1] inputs to determine the next action. During the correlate mode, the Controller activates the PA, WFG and Correlator subsystems so that the data stream from the FEMs can be phase-aligned and correlations can be performed by asserting INTEGRATE. The PA and WFG are activated by asserting PA_RES/COR_RES and WFG_RES, respectively. A timer is used to control the integration period by counting clock pulses on COR_CLK. When it times-out, the Controller deasserts INTEGRATE, turns off the PA by deasserting PA_RES/COR_RES, turns off the WFG by deasserting WFG_RES and enters output mode.

In output mode, the Controller asserts LOAD_EN/READ to allow the correlation products to be strobed into the ODF. The strobing action is effected by toggling CS. Once the ODF is loaded the Controller sets the STATUS outputs to indicate DATAVAIL. SEDS reads the data by handshaking with the ODF as discussed in [2]. The number of products transferred to SEDS is under the control of a state machine to be discussed below. When the

appropriate number of products has been transferred, the mode is changed to either calibrate or correlate, alternately, as discussed in Section 2.

Calibrate mode is identical to correlate mode except that the source of the FEM input signals is the on-board calibration source. In this mode, CALTAG is asserted and is used to effect the switching to the calibration source. Once calibrate mode is completed, output mode is entered.

In test mode, the ODF and WFG are exercised to determine their level of functionality. Testing of the ODF involves the generation in the Controller of a 3-bit pseudo-noise code sequence. This data is placed on TODF_OUT and strobed into the ODF using TODF_CLK. As discussed in [2], the data is circulated throughout the ODF and is returned to the Controller on ODF_TIN. In the Controller it is compared with the original data. A discrepancy indicates a circuit fault in the ODF, and the Controller indicates this fact by setting the ERRODF status bits.

Testing of the WFG involves use of walsh function generation circuitry inside the Controller to generate test data. Output WFG_CLK is toggled to cause the WFG to generate function values, which are read by the Controller on WFG_TIN. The data is compared with the internally generated values and if there is a mismatch the Controller sets the ERRWFG status bits. Once both the WFG and ODF are tested, the DDS Controller enters command mode.

### 3.3 Internal Details

The architecture of the Controller is depicted in Figure 4. In the figure, subsystems

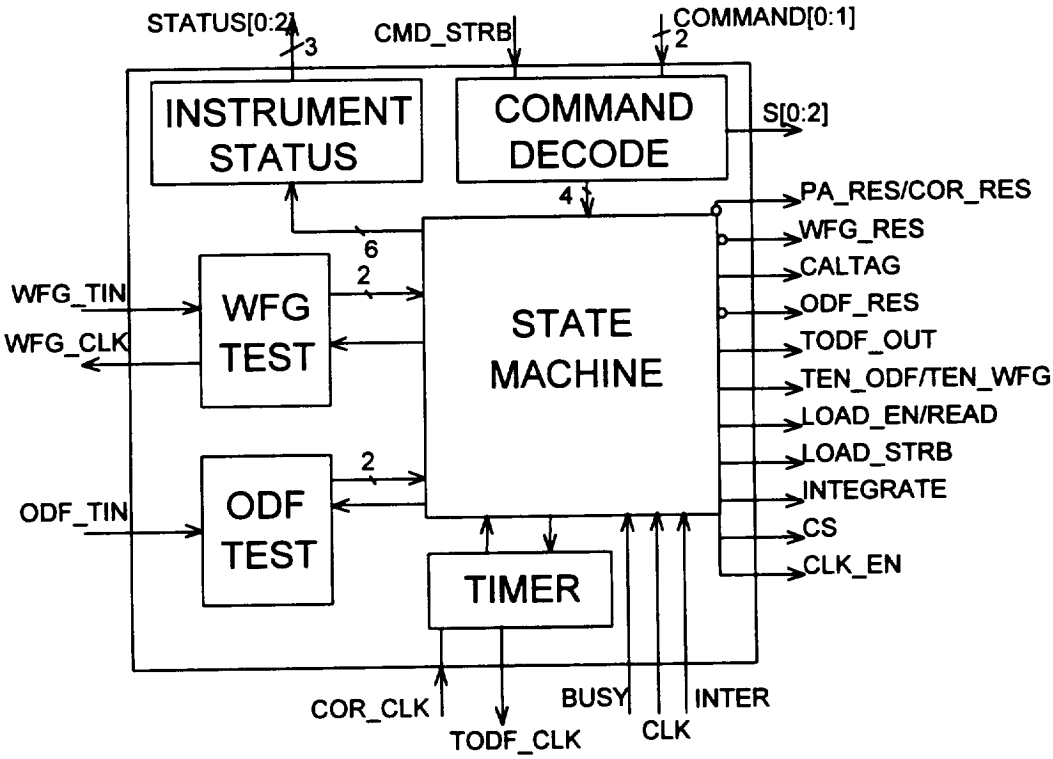



Figure 4: DDS Controller Functional Block Diagram

ODF Test and WFG Test contain the test circuitry for the ODF and WFG, respectively. They include the three bit pseudo-random noise generator and walsh function generator discussed above. WFG Test includes circuitry to generate the test clock for the WFG.

Instrument Status is a 6-to-3 encoder which uses a standard architecture consisting of three 6-input OR gates to encode the instrument status lines. Command Decode is a 2-to-4 decoder with registered inputs which uses a standard architecture consisting of 4 two-input AND gates to decode SEDS commands for the Controller. It also contains circuitry which latches the identification code bits during the test command.

The Timer controls the length of the correlation period and flags the State Machine when the period is finished.

The State Machine performs the control operations. For example, it tracks the mode of operation and determines which outputs are active at any given time. Its operation will now be discussed.

The State Machine is an 11-input, 20-output, eight state synchronous design whose bubble diagram is given in Figure 5.

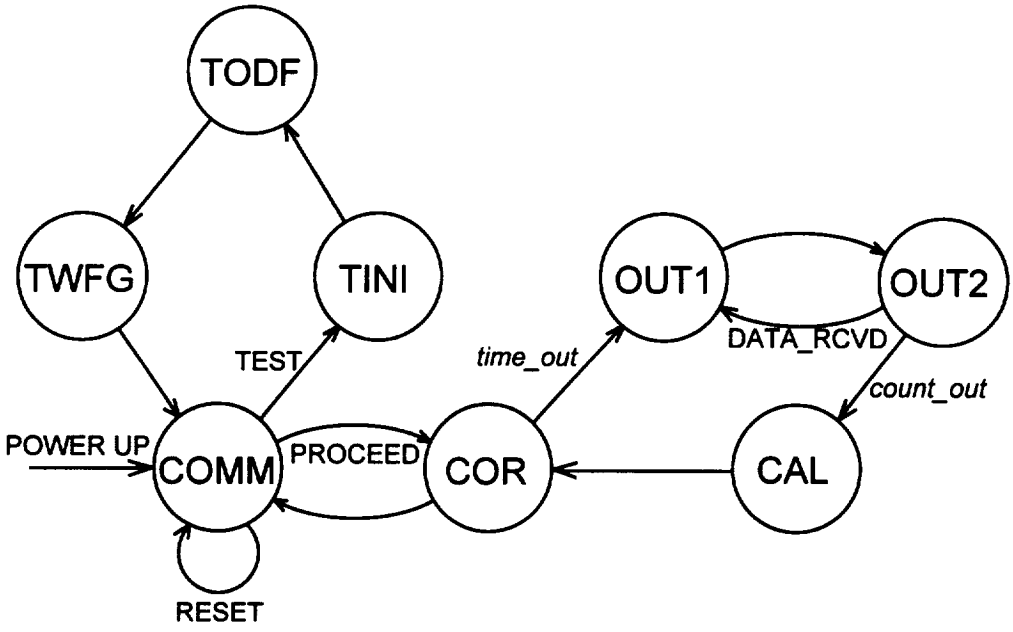



Figure 5: Bubble Diagram of State Machine

The states of the machine are:

COMM: "Reset" state in which the command decode subsystem (see Figure 4) is observed and action is taken according to its contents. Corresponds to command mode.

TINI: Test mode initialization state during which the ODF and WFG are set for test mode operation.

TODF: The state during which the ODF is tested.

TWFG: The state during which the WFG is tested.
COR: This state corresponds to both correlate and calibrate modes. It begins by initializing the internal registers of the Correlator. It then Initiates the data transfer from the FEMs to the Correlator by asserting the PA (i.e., asserting PA_RES/COR_RES). Correlation is performed by asserting the Timer and INTEGRATE of the Correlator, while also enabling the WFG by asserting WFG_RES. Upon timeout of the Timer (signal *time_out* in the figure), INTEGRATE is deasserted and data flow from the PA is stopped by deasserting PA_RES/COR_RES. The WFG is disabled by deassertion of WFG_RES, and state OUT1 is entered.
OUT1: This state is the first of two that correspond to output mode. In this state, the correlation products are placed in the ODF by strobing LOAD_EN/READ and toggling CS. SEDS is informed that data is available by the assertion of the DATAVAIL status code.
OUT2: SEDS serially reads the correlation product from the ODF using the handshaking protocol discussed in [2]. When SEDS informs the Controller that the data word was received (i.e., by sending the command DATA_RCVD), then the Controller returns to state OUT1 so that the next data word can be placed in the ODF. Alternation between states OUT1 and OUT2 continues for 7600 products, which is the number of complex correlation products needed for a full ESTAR mission with 124 dipoles. When all products have been passed to SEDS (indicated by signal *count_out* in the figure), state CAL is entered.
CAL: This state switches the source of the FEM data to the onboard calibration source by asserting CALTAG. Control is then transferred to state COR. This state corresponds to the first of two calibrate mode states. COR is the other.

## 4. Specifications

### 4.1 Electrical Specifications

Maximum Absolute Ratings:

| Symbol | Description | Value | Units | Conditions |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -.5 to +7.0 | V | |
| $V_{in}$ | Input Voltage | -.5 to $V_{cc}$+.5 | V | |
| $V_{TS}$ | Tri-state applied voltage | -.5 to $V_{cc}$+.5 | V | |
| $T_{STG}$ | Storage Temperature | -65 to +150 | Degrees Centigrade | |
| $T_{SOL}$ | Max. Soldering Temperature | +260 | Degrees Centigrade | |
| $T_J$ | Junction Temperature | +125 | Degrees Centigrade | |

Recommended Operating Conditions:

| Symbol | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage 0°C to 70°C | 4.75 | 5.25 | V | |
| $V_{IHT}$ | TTL High-Level Input | 2.0 | Vcc | V | |
| $V_{ILT}$ | TTL Low-Level Input | 0 | 0.8 | V | |
| $V_{IHC}$ | CMOS High-Level Input | 70% | 100% | V | |
| $V_{ILC}$ | CMOS Low-Level Input | 0 | 20% | V | |
| $T_{IN}$ | Input Transition Time | | 250 | ns | |

DC Characteristics Over Operating Conditions:

| Symbol | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $V_{OH}$ | High-Level Output Voltage | 3.86 | | V | $I_{OH}$= 4.0mA $V_{CC}$ min |
| $V_{OL}$ | Low-Level Output Voltage | | .32 | V | $I_{OL}$=4.0 mA $V_{CC}$ max |
| $V_{CCPD}$ | Power-Down Supply Voltage | 2.3 | | V | |
| $I_{CCPD}$ | Power-Down Supply Current | | 120 | µA | $V_{CC}$ max T max |
| $I_{IL}$ | Input Leakage Current | -10 | +10 | µA | |
| $C_{IN}$ | Input Capacitance | | 10 | pF | Sample Tested |

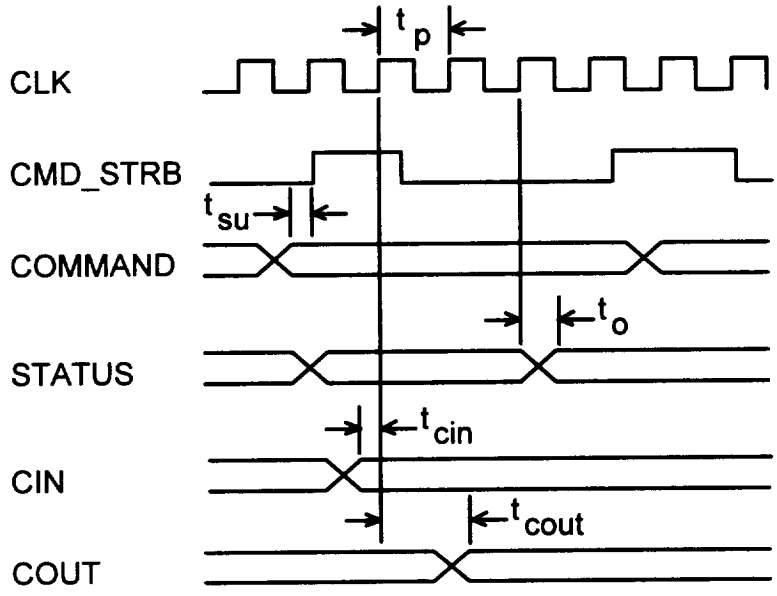
AC Electrical Characteristics Over Operating Conditions:

| Symbol | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $t_{rise}$ | Input rise time | | 250 | ns | Worst case[1] |
| $t_{fall}$ | Input fall time | | 250 | ns | Worst case[1] |
| $t_{cin}$ | Setup time for any control input | 55.4 | | ns | Worst case[1] |
| $t_p$ | Clock period | 100 | | ns | Worst case[1] |
| $t_{cout}$ | CLOCK to valid control outputs | | 37.1 | ns | Worst case[1] |
| $t_{su}$ | Setup time of COMMAND to CMD_STRB | 14.6 | | ns | Worst case[1] |
| $t_o$ | CLK edge to valid STATUS data | | 42.1 | ns | Worst case[1] |
| f | Clock frequency | | 10 | MHz | Worst Case[1] |

Notes:

1) 70° C and 4.75 volt supply.

Timing Diagram:



## 4.2 Schematic

The schematic diagram of the Controller prototype is shown in Figure 6.

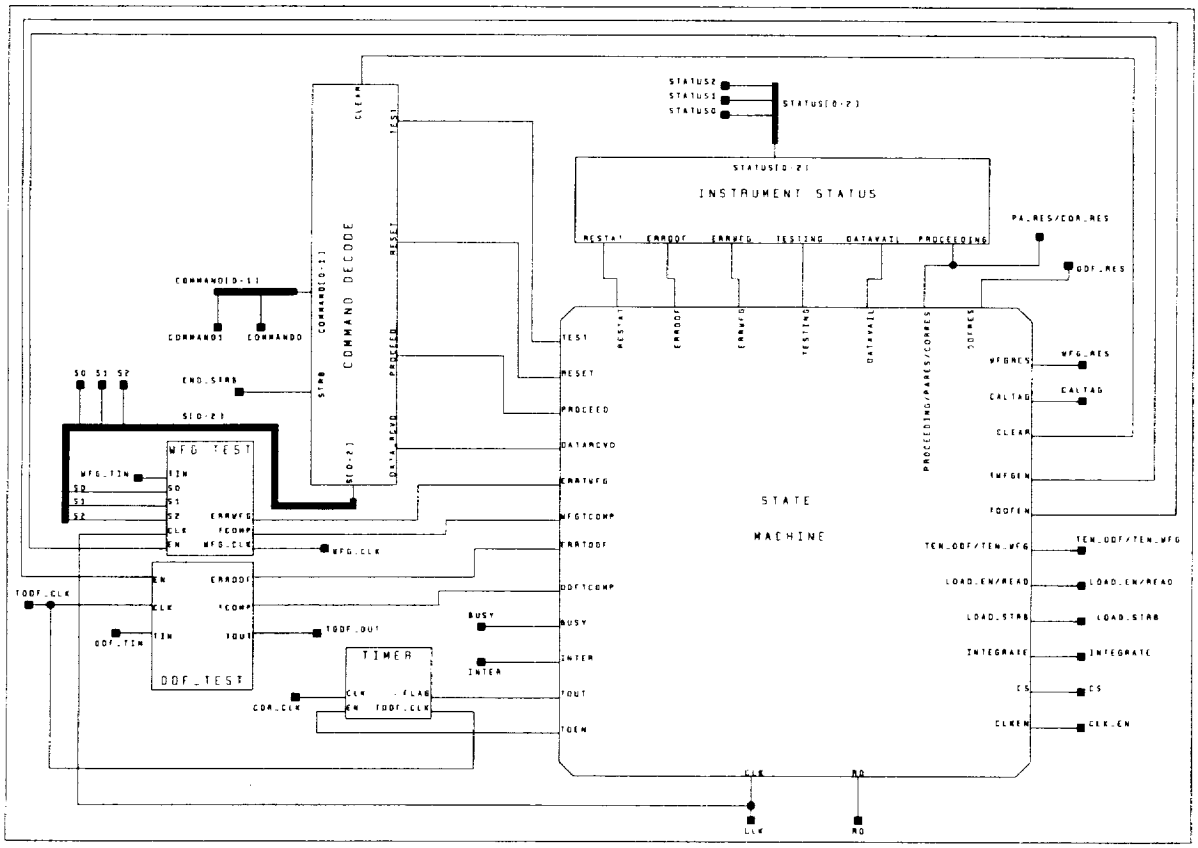



Figure 6: DDS Controller Prototype Schematic Diagram

## 5. Signal Descriptions

### 5.1 Control Inputs

| | |
|---|---|
| COMMAND[0:1] | Two control bits that determine Controller's mode of operation; come from SEDs |
| CLK | Clock signal for the Controller; must have frequency one-half that of COR_CLK |
| CMD_STRB | Strobes commands from SEDS into Controller on low-to-high transition |

| | |
|---|---|
| BUSY | Asserted high by Correlator during correlation and when data remains to be read from the Correlator |
| INTER | Asserted low when Correlator data is available for reading; high immediately after the first data word has been read |

**5.2 Control Outputs**

| | |
|---|---|
| STATUS[0:2] | Three control bits that indicate the status of the Controller; used by SEDS |
| PA_RES/COR_RES | Asserted low to enable the Phase Aligner and Correlator |
| WFG_RES | Asserted low to enable the WFG |
| CALTAG | Asserted high to indicate calibrate mode and to switch the FEM inputs to on-board calibration sources |
| ODF_RES | Asserted low to enable the ODF |
| TEN_ODF/TEN_WFG | Asserted high to set the ODF and WFG into test mode |
| LOAD_EN/READ | Asserted high to enable the ODF to be parallel loaded with data from the Correlator; also enables reading of the data in the Correlator |
| LOAD_STRB | A low-to-high transition causes a parallel load of the ODF |
| INTEGRATE | Asserted high to start the integration process in the Correlator |
| CS | Select control pin for the Correlator; rising edge allows correlation products to be read from the output bus |
| CLK_EN | Asserted high to enable the System Clock |
| WFG_CLK | Clock for the WFG |
| TODF_CLK | Test clock for the ODF |
| COR_CLK | Clock signal for Correlator; frequency must be twice that of CLK |

### 5.3 Data Inputs

| | |
|---|---|
| WFG_TIN | Input for test data from the WFG |
| ODF_TIN | Input for test data from the ODF |

### 5.4 Data Outputs

| | |
|---|---|
| TODF_OUT | Test data from the pseudo-random noise generator which is used to test the ODF during test mode |
| S0,S1,S2 | Data bits from test command; set Walsh range |

## 6. Package Type

The DDS Controller prototype is implemented in an 84-pin PLCC package with a speed grade of 100 MHz (part number XC3064PC84-100). The FPGA gate density is 62% (139/224 available CLBs used); the pin density is 40% (28/70 available IOBs used).

## 7. References


[1] Levine, D. M., Hilliard, L., et. al., 1990, *Electronically Scanned Thinned Array Radiometer (ESTAR) Earth Probe Concept: An Engineering Feasibility Analysis*, Goddard Space Flight Center, page 9.

[2] Chren, W. A., Jr., 1993, *Output Data Formatter for the ESTAR Instrument*, NASA Technical Memorandum #TM-4432.

[3] Chren, W. A., Jr., 1993, *Walsh Function Generator for the ESTAR Instrument*, NASA Technical Memorandum #TM-4449.

[4] Chren, W. A., Jr., Zomberg, B.G., 1993, *Phase Aligner for the Electronically Scanned Thinned Array Radiometer (ESTAR) Instrument*, NASA Technical Memorandum #TM-4518.

[5] Levine, D. M., Good, J. C., 1983, "Aperture Synthesis for Microwave Radiometers in Space", NASA TM 85033, page 1.

[6] Levine, D. M., Gatlin, J., et. al., *Peer Review of LaRC Six-Month Study of "ESTAR" Small S/C Mission*, Langley Research Center/Goddard Space Flight Center internal document, 10/9/92.

[7] Chren, W. A., Jr., *A Digital Data Subsystem Design for an L-band ESTAR Instrument: A Summary of Research Performed in the JOVE Fellowship Program, 6/1/91 through 11/30/91,*

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**13. ABSTRACT** *(Maximum 200 words)*

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